	Search Text
1	fpga and (peripheral proprietary custom$5 specific) near2 function and rom and (user engineer designer) with access$4 and @ad<"20011210"
2	fpga and (peripheral proprietary custom$5 specific) near2 function and rom and (user engineer designer) with access$4 and @ad<"20011210" and register and peripheral
3	fpga and (peripheral proprietary custom$5 specific) near2 function and rom and (user engineer designer) with access$4 and @ad<"20011210" and register and peripheral and (por power near2 reset$4)
4	fpga and (peripheral proprietary custom$5 specific) near2 function and rom and (user engineer designer) with access$4 and @ad<"20011210" and register and peripheral and (por power near2 reset$4)
5	fpga and (peripheral proprietary custom$5 specific) near2 function and rom and (user engineer designer) with access$4 and @ad<"20011210" and register and peripheral and (por power near2 reset$4) and bus$4
6	fpga and (peripheral proprietary custom$5 specific) near2 function and rom and (user engineer designer) with access$4 and @ad<"20011210" and peripheral and (por power near2 reset$4)
7	fpga and (peripheral proprietary custom$5 specific) near2 function and rom and (user engineer designer) with access$4 and @ad<"20011210" and peripheral and (por power near2 reset$4) and bus$5
8	fpga and (peripheral proprietary custom$5 specific) near2 function and rom and (user engineer designer) with access$4 and @ad<"20011210" and peripheral and (por power near2 reset$4) and bus$5 with (processor cpu local peripheral)
9	fpga and (peripheral proprietary custom$5 specific) near2 function and rom and (user engineer designer) with access$4 and @ad<"20011210" and peripheral and (por power near2 reset$4) and bus$5 with (processor cpu local peripheral) and (arbit$4 uart bridge controller)
10	fpga and (peripheral proprietary custom$5 specific) near2 function and rom and (user engineer designer) with access$4 and @ad<"20011210" and peripheral and (por power near2 reset$4) and bus$5 with (processor cpu local peripheral) and (arbit$4 uart bridge) and controller
11	fpga and (peripheral proprietary custom$5 specific) near2 function and rom same (peripheral proprietary custom$6 specific)and (user engineer designer) with access$4 and @ad<"20011210" and peripheral and (por power near2 reset$4) and bus$5 with (processor cpu local peripheral) and (arbit$4 uart bridge) and controller
12	fpga and (peripheral proprietary custom$5 specific) near2 function and rom same (peripheral proprietary custom$6 specific) and (user engineer designer) with access$4 and @ad<"20011210" and peripheral and (por power near2 reset$4) same (peripheral proprietary custom$6 specific) and bus$5 with (processor cpu local peripheral) and (arbit$4 uart bridge) and controller
13	(system-on-chip or soc or system adj2 chip embed$5) and (user customer designer engineer) same (fpga or (peripheral proprietary custom$5 specific) near2 function) same access$4 and @ad<"20011210" and (por power near2 reset$4) same (peripheral proprietary custom$6 specific fpga)

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14	(system-on-chip or soc or system adj2 chip embed$5) and (user customer designer engineer) same (fpga or (peripheral proprietary custom$5 specific) near2 function) same access$4 and @ad<"20011210" and (por power near2 reset$4) same (peripheral proprietary custom$6 specific fpga) and rom
15	(system-on-chip or soc or system adj2 chip embed$5) and (user customer designer engineer) same (fpga or (peripheral proprietary custom$5 specific) near2 function) same access$4 and @ad<"20011210" and (por power near2 reset$4 power-on) same (peripheral proprietary custom$6 specific fpga) and rom
16	(system-on-chip or soc or system adj2 chip embed$5) and (user customer designer engineer) same (fpga or (peripheral proprietary custom$5 specific specialized) near3 function) same access$4 same (allow$7 enabl$5) and @ad<"20011210" and (por power near2 reset$4 power-on) same (peripheral proprietary custom$6 specific fpga) and rom
17	(system-on-chip or soc or system adj2 chip embed$5) and (user customer designer engineer) same (fpga or (peripheral proprietary custom$5 specific specialized) near3 function) same access$4 same (allow$7 enabl$5) and @ad<"20011210" and (por power near2 reset$4 power-on near3 reset$4) same (peripheral proprietary custom$6 specific fpga) and rom
18	(system-on-chip or soc or system adj2 chip embed$5) and (user customer designer engineer) same (fpga or (peripheral proprietary custom$5 specific specialized) near3 function) same access$4 same (allow$7 enabl$5) and @ad<"20011210" and (por power near2 reset$4 power-on near3 reset$4) same (peripheral proprietary custom$6 specific fpga) and rom and ((data bit) adj (string stream) or datastream or datastring or bit stream or bitstring)
19	(user customer designer engineer) same (fpga or (peripheral proprietary custom$5 specific specialized) near3 function) same access$4 same (allow$7 enabl$5) same (por power near2 reset$4 power-on near3 reset$4) and @ad<"20011210" and rom and ((data bit) adj (string stream) or datastream or datastring or bit stream or bitstring)
20	fpga and (block cell) same configur$6 same (customer user designer engineer) and @ad<"20011210"
21	fpga and (block cell macro$6) same configur$6 same (customer user designer engineer) and @ad<"20011210"
22	fpga and (block cell macro$6) same configur$6 same (customer user designer engineer) and @ad<"20011210" and (por power near2 reset$4 power-on near3 reset$4) and rom$4
23	fpga and (block cell macro$6) same configur$6 same (customer user designer engineer) and @ad<"20011210" and (por power near2 reset$4 power-on near3 reset$4) and rom
24	fpga and (block cell macro$6) same configur$6 same (customer user designer engineer) and @ad<"20011210" and (por power near2 reset$4 power-on near3 reset$4) and rom and (customer user designer engineer) same (enabl$4 allow$7) same access$6
25	(system-on-chip or soc or system adj2 chip embed$5) and fpga and (block cell macro$6) same configur$6 same (customer user designer engineer) and @ad<"20011210" and (por power near2 reset$4 power-on near3 reset$4) and rom and (customer user designer engineer) same (enabl$4 allow$7) same access$6

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26	(system-on-chip or soc or system adj2 chip embed$5) and fpga and (block cell macro$6) same configur$6 same (customer user designer engineer) and @ad<"20011210" and (por power near2 reset$4 power-on near3 reset$4) and rom and (customer user designer engineer) same (enabl$4 allow$7) same access$6 and peripheral
27	(system-on-chip or soc or system adj2 chip embed$5) and fpga and (block cell macro$6) same configur$6 same (customer user designer engineer) and @ad<"20011210" and (por power near2 reset$4 power-on near3 reset$4) and rom and (customer user designer engineer) same (enabl$4 allow$7) same access$6 and peripheral and bus$4
28	(system-on-chip or soc or system adj2 chip embed$5) and (user customer designer engineer) same (cell block macro$4) same access$4 same (allow$7 enabl$5) and @ad<"20011210" and (por power near2 reset$4 power-on near3 reset$4) and rom and ((data bit) adj (string stream) or datastream or datastring or bit stream or bitstring)
29	fpga and (system-on-chip or soc or system adj2 chip embed$5) and (user customer designer engineer) same (cell block macro$4) same access$4 same (allow$7 enabl$5) and @ad<"20011210" and (por power near2 reset$4 power-on near3 reset$4) and rom and ((data bit) adj (string stream) or datastream or datastring or bit stream or bitstring) and (cell block macro$4) same register
30	fpga and (system-on-chip or soc or system adj2 chip embed$5) and (user customer designer engineer) same (core ip) same access$4 same (allow$7 enabl$5) and @ad<"20011210" and (por power near2 reset$4 power-on near3 reset$4) and rom and ((data bit) adj (string stream) or datastream or datastring or bit stream or bitstring) and (cell block macro$5 core ip) same register
31	fpga and (soc syetem-on embedded) same (macro$4 cell block core) same (enable allow$4) same (peripheral)
32	fpga and (soc system-on embedded) same (macro$4 cell block core) same (enable allow$4) same (peripheral)
33	fpga and (soc system-on embedded) same (macro$4 cell block core) same (enable allow$4) same (peripheral) and @ad<"20011210"
34	fpga and (soc system-on embedded) same (macro$4 cell block core) same (enable allow$4) same (dedicat$4 custom$4 specific) same function and @ad<"20011210"
35	fpga and (soc system-on embedded) same (macro$4 cell block core) same (enable allow$4) same (dedicat$4 custom$4 specific) same function and @ad<"20011210" and rom
36	fpga and (soc system-on embedded) same (macro$4 cell block core) same (enable allow$4) same (dedicat$4 custom$4 specific) same function and @ad<"20011210" and rom and (por power near2 reset$4 power-on near3 reset$4)